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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,785	08/31/2001	Ming-Dou Ker	0941-0322P-SP	9752
2292	7590	03/04/2004	EXAMINER	
BIRCH STEWART KOLASCH & BIRCH PO BOX 747 FALLS CHURCH, VA 22040-0747			KITOV, ZEEV	
			ART UNIT	PAPER NUMBER
			2836	

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/942,785

Applicant(s)

KER ET AL.

Examiner

Zeev Kitov

Art Unit

2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 31 August 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4 - 18, 21, 22 is/are rejected.
- 7) ☒ Claim(s) 3, 19 and 20 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 31 August 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "a forth NMOS component and a fifth NMOS component, connected in series between the pad and I/O low power line" (see Claim 21), must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claim 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. A reason for that is the following statement of the claim: "a forth NMOS component and a fifth NMOS component, connected in series between the pad and I/O low power line". The circuit according to the claim language is not disclosed in Specification, neither in Drawings. The circuit structure (transistors Mp7, Mn7) shown

in Fig. 8, 9, 12 and 13 does not include two transistors connected in series between the I/O pad and the ground.

For purpose of examination the structure was assumed according to the Drawings and “the PMOS connected between I/O pad and the high power supply terminal having its gate connected to the high power line and NMOS connected between the I/O pad and the low power line having its gate connected to the low power supply line”. Appropriate explanation/correction is required.

Objections

Claim 18 is objected to due to a minor error: “a first source/drain coupled the pad” should be corrected as: “a first source/drain coupled to the pad”.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4 - 6, 8 - 12, 15 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Puar (US 5,287,241). Puar discloses all the elements of Claims 1 including electrostatic discharge (ESD) protection circuit for an integrated circuit (IC), the ESD protection circuit including: an ESD clamp device (elements D3 and D4 in Fig.4), coupled to a pad (element T2 in Fig.4) and a substrate having a first conductivity

type (see Fig. 5, col. 7, lines 24-57), the ESD clamp device being closed under normal power operation; and a functional component (elements N2, P2 in Fig. 4 and 5), formed on the substrate and coupled to the pad, the functional component having a first well of the first conductivity type (p-type drain well in Fig. 5) and an isolating region of a second conductivity type N-type well in Fig.5), the second conductivity type being the reversed polarity of the first conductivity type, and the isolating region isolating the first well from the substrate; the functional component transmitting signals between the IC and an external linkage under normal power operation.

Regarding Claims 9 and 15, Puar discloses an MOS component having second conductivity type (elements N1 and N2 in Fig. 4 and 5). Regarding Claim 9 limitations, the first MOS component (element N1 in Fig. 4) transmits signals from the pad into the IC. As to this MOS structure, it is inherently the same as the structure of N2 transistor, because in the integrated circuits similar elements always built similar way. As to the Claim 15 limitations, transistor N2 represents the MOS component of the claim.

Regarding Claim 4, Puar discloses the functional component including a metal-oxide semiconductor (MOS) (element N2 in Fig. 4) having the second conductivity type in the first well (see Fig. 5).

Regarding Claim 5, Puar discloses the ESD clamp device including an MOS diode (elements D3 and D4 in Fig. 4) having two ends respectively coupled to the pad and the substrate (see Fig. 5).

Regarding Claim 6, Puar discloses a two-stage ESD protection circuit having a primary ESD protection circuit (element D1 and D2 in Fig. 4) coupled between the pad

and the substrate, a secondary ESD protection circuit coupled between the functional component (elements D3 and D4 in Fig. 4) and the substrate, and a resistor (element R2 in Fig. 4) coupled between the functional component and the pad (element T2 in Fig. 4). As to connection to the substrate, Puar discloses that the Vss line of the supply is connected to the substrate (col. 1, lines 41 –57).

Regarding Claim 8, Puar discloses the first conductivity type as an N type, and the second conductivity type as p type (see Fig. 5).

Regarding Claim 10, Puar discloses the gate of the MOS component (element N1 in Fig. 4) being coupled to the pad (T1 input in Fig. 1).

Regarding Claim 11, Puar discloses the source of the MOS component is coupled to an internal power line (source of the element N1 in Fig. 4 is grounded).

Regarding Claim 12, Puar discloses the ESD protection circuit (elements D1 and D2 in Fig. 1) coupled between the gate of the MOS component and the internal power lines (VDD and VSS in Fig. 1).

Regarding Claim 16, Puar discloses the drain of the MOS component (element N2 in Fig. 4) coupled to the pad and a source of the MOS component and the first well associated with the source are coupled to an I/O power line (VSS in Fig. 4).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Puar in a view of Poplevine et al. (US 6,184,557). As was stated above, Puar discloses all the elements of Claim 1. However, regarding Claim 2, it does not disclose the isolating region having a second well surrounding the first well and a deep well under the first well. Poplevine et al. disclose the functional element structure with the isolating region having a second well (elements 424 and 426 in Fig. 4) surrounding the first well and a deep well under the first well (element 516 in Fig. 4, col. 4, lines 36 – col. 5, line 65). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Puar solution by adding the second well and the deep well according to Poplevine et al., because as Poplevine et al. state (col. 3, lines 27 – 34), such a structure would provide more balanced capacitances and resistances and therefore, more symmetric outputs.

Claims 7, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puar in a view of Watt (US 5,477,413). As was stated above, Puar discloses all the elements of Claim 1. However, regarding Claim 7, it does not disclose the first conductivity type as an N type, and the second conductivity type as p type. Watt discloses an electrostatic discharge (ESD) protection circuit having the first conductivity type as an N type, and the second conductivity type as p type (see Fig. 5). Both patents have the same problem solving area, namely providing the ESD protection circuit in

integrated circuit form. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Puar solution by changing the type of material conductivity from "P" to "N" and vice versa, according to Watt, because as Watt states (col. 9, lines 24 – 34), that his invention can be implemented by a triple well processing (which is usually) a p-well placed into an n-well which itself is in a p-substrate. Thus he suggests that the two technologies are interchangeable. Selection of particular technology is up to the designer.

Regarding Claim 13, Watt discloses the ESD protection circuit at the input port as a gate-grounded MOS component (elements 34 – 37 in Fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Puar solution by adding the ESD input protection element according to Watt, because as Watt states (col. 3, line 56 – col. 6, line 19), such solution provides very low threshold clamp (see Fig. 2B) capable of protecting the circuits fed by low voltages.

Regarding Claim 14, Watt discloses the first well (element 57f in Fig. 5) being coupled to the internal power line (element VSS in Fig. 5). A motivation for modification of the primary reference is the same as above.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Puar in a view of Maloney (US 5,530,612). As was stated above, Puar discloses all the elements of Claim 15. However, regarding Claim 17, it does not disclose a plurality of diodes. Maloney discloses the plurality of diodes disposed between the I/O power line

and the internal power line (elements 21 – 24 in Fig. 10a, col. 10, lines 1 – 15).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Puar solution by adding the strings of diodes according to Maloney, because as Maloney states (col. 10, lines 1 – 15, col. 8, lines 17 – 30), the diodes are necessary to protect the I/O terminal from positive or negative zapping.

Claims 18 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puar (US 5,287,241) in a view of Adams et al. (US 4,782,250) and further in a view of Waggoner (US 5,917,220). Regarding Claim 18, Puar discloses following elements: electrostatic discharge (ESD) protection circuit for an integrated circuit (IC), the ESD protection circuit including: an ESD clamp device (elements D3 and D4 in Fig.4) coupled to a pad (element T2 in Fig.4) and a p-type substrate (see Fig. 5, col. 7, lines 24-57), the ESD clamp device being closed under normal power operation; and a first NMOS component (elements N1 and N2 in Fig. 4 and 5) formed on the substrate and coupled to the pad, the functional component having a first well of the first conductivity type (p-type drain well in Fig. 5) and an isolating region of a second conductivity type N-type well in Fig.5), the second conductivity type being the reversed polarity of the first conductivity type, and the isolating region isolating the first well from the substrate; the functional component transmitting signals between the IC and an external linkage under normal power operation.

However, it discloses neither an output driver, nor the first NMOS having their NMOS gates connected to a high power line.

Waggoner discloses the functional component transmitting signals between the IC and an external linkage under normal power operation, which includes MOSFET (element T3 in Fig. 8), having its gate connected to the high power line (VDD in Fig. 8). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have modified the Puar solution by adding the dropping transistor having its gate connected to the high power line according to Waggoner, because as Waggoner states (col. 8, lines 32 – 37), it would reduce the voltage at the input node to protect the more sensitive CMOS transistors.

Adams et al. disclose an output driver including a second and a third NMOS component respectively (elements 26 and 22 in Fig. 1) formed in a P-type second isolated well on the substrate and connected in series; an N-type second isolating region formed between the P-type second isolated well and the substrate (see Fig. 2), a gate of the second NMOS component (element 26 in Fig. 1), coupled to the high Power line, its drain is coupled to the pad, and its source is coupled to a drain of the third NMOS component, which source is coupled to an I/O low power line (ground), and a gate of the third NMOS component is being coupled to a pre-output driver (elements 14 and 16 in Fig. 1). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Puar solution by adding the dual cascaded transistors structure according to Adams et al., because as Adams et

al. state (col. 5, lines 25 – 28), such structure would help to avoid excessive gate oxide stress on the pull down transistors (element 22 in Fig.1).

Regarding Claim 22, Puar discloses the ESD protection resistor (element R1 in Fig. 4) formed between the first NMOS component (element N1 in Fig. 4) and the pad.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Puar in a view of Adams et al. and Waggoner and further in a view of Watt. As was stated above, Puar, Adams et al. and Waggoner disclose all the elements of Claim 18. However, regarding Claim 21, they do not disclose the PMOS connected between I/O pad and the high power supply terminal having its gate connected to the high power line and NMOS connected between the I/O pad and the low power line having its gate connected to the low power supply line (see Rejection under USC 112 above). Watt discloses protection against positive ESD accomplished by NMOS transistors having their gates coupled to the low power line (elements 25, 26 in Fig. 2A) and connected between the I/O pad and the low power line. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Puar solution by adding the NMOS circuit protection against positive ESD events according to Watt, because as Watt states (col. 2, lines 10 – 15), unlike the diode, such structure would conduct only if sufficiently strong ESD event is applied. Additionally, a similar circuit for protection against negative ESD events must be added. Such circuit would be PMOS analog of the Watt structure. It would have PMOS transistor connected between the I/O pad and the high power line with its gate

connected to the high power line. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further modified the Puar solution by adding the PMOS analog of the Watt circuit, because as Watt states (col. 1, lines 50 – 53), the circuit must be protected from both positive and negative ESD events.

Allowable Subject Matter

Claims 3, 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. A reason for that is that Claims 3 and 19 recite the isolating region is coupled to a first power supply and the first well is coupled to a second power supply. This feature was not found in the collected prior art of the record.

Conclusion

The prior art made of record not relied upon is considered pertinent to applicant's disclosure: US 6,049,119, US 6,046,897, US 6,594,132.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose current telephone number is (571) 272 - 2052. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can

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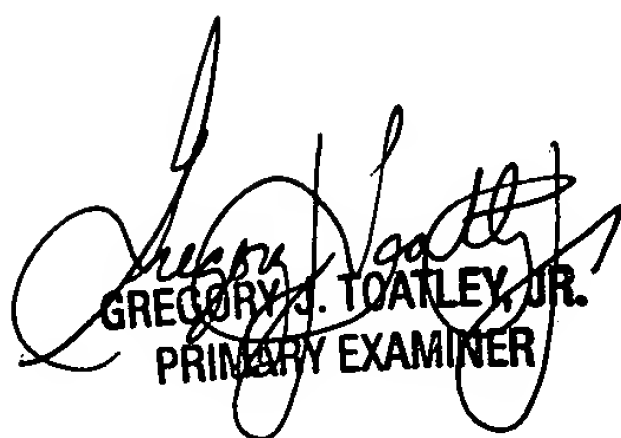
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be reached on (571) 272 – 2800, Ext. 36. The fax phone number for organization where this application or proceedings is assigned is (703) 872-9306 for all communications.

Z.K.

02/16/2004


GREGORY J. TOATLEY, JR.
PRIMARY EXAMINER